COMPENSATION CIRCUIT FOR AMPLIFIERS
HAVING MULTIPLE STAGES

FIELD OF THE INVENTION

[0001]   The present invention relates to amplifiers, and more particularly to compensation circuits for amplifiers having two or more stages.

BACKGROUND OF THE INVENTION

[0002]   Referring now to FIG. 1, an amplifier circuit 10 without compensation is shown.   A voltage source V_i delivers voltage through an impedance Z_1 to an inverting input of an amplifier 16. A non-inverting input of the amplifier 16 is coupled to a reference potential such as ground.   The inverting input of the amplifier 16 is coupled through a feedback impedance Z_2 to an output of the amplifier 16.   A load capacitance C_L is coupled to the output of the amplifier 16.   An output voltage V_O is taken at the output of the amplifier 16. The impedances Z_1 and Z_2 can be resistive, capacitive and/or short circuits.

[0003]   Because power supply voltage levels have been reduced to decrease the power dissipation of a host device, it has become more difficult to supply voltage to the required transistors when they are arranged in a single amplifier stage. Therefore, the amplifier 16 is sometimes implemented using two or more amplifier stages.   When two or more stages are required, compensation is also typically required to increase the gain and/or bandwidth of the amplifier circuit.

[0004]   Referring now to FIGs. 2A and 2B, a two stage amplifier circuit 18 with Miller compensation is shown. The amplifier 16 includes a first amplifier stage 20 having a first transconductance g_{m1} and a second amplifier stage 22 having a second transconductance g_{m2}. The output of the first amplifier stage 20 is connected to an inverting input of the second amplifier stage 22. Compensation is provided by a Miller capacitor C_m having one end that is connected to the input of the second amplifier stage 22. Another end of the Miller capacitor C_m is connected to the output of the second amplifier stage 22.

[0005]   The most relevant characteristics of an amplifier circuit are gain and bandwidth. The following discussion sets forth the open loop DC gain and the bandwidth of the circuit in FIG. 2B both with and without the Miller capacitance C_m. To correctly identify the bandwidth, a parasitic capacitance C_p of the second amplifier stage 22 and internal resistances R_1 an R_2 of the first and second amplifier stages 20 and 22 are considered as shown in FIG. 2B.

[0006]   In order to derive the bandwidth, an open loop response technique is used. The open loop response technique provides information relating to the bandwidth and maximum achievable bandwidth of a circuit. The DC gain of the open loop response is determined by opening the feedback loop adjacent to the output of the second amplifier stage and attaching a voltage source to one end of the feedback loop. The output voltage is sensed at the other end of the feedback loop as shown in FIG. 2B.

[0007]   To derive the bandwidth, the DC gain of the open loop response and the first dominant pole P_1 are found. Assuming stable operation, there is

only one pole P_1 that is located below a crossover frequency. The crossover frequency is the product of the DC gain of the open loop response and the first dominant pole P_1. The crossover frequency defines the bandwidth of the closed loop amplifier. The maximum available bandwidth is related to the second non-dominant pole P_2.

[0008]   Referring now to FIG. 3, the response of the amplifier circuit of FIG. 2B without the Miller compensation capacitor C_m is shown. The DC gain of the open loop response is $\dfrac{Z_1}{Z_1 + Z_2} g_{m1} R_1 g_{m2} R_2$ and the circuit has a first pole at $\dfrac{1}{C_P R_1}$ and a second pole at $\dfrac{1}{C_L R_2}$. The first and second poles occur at frequencies that are relatively close together. The dominant pole of the first and second poles will depend upon the values of C_L, C_P, R_1 and R_2.

[0009]   Referring now to FIG. 4, the response of the amplifier circuit of FIG. 2B with the Miller compensation capacitor C_m is shown. The DC gain of the open loop response is the same as the amplifier circuit without the Miller compensation capacitor C_m. The circuit has a dominant pole at $\dfrac{1}{(C_P + C_m A_2)R_1} = \dfrac{1}{(C_P + C_m g_{m2} R_2)R_1}$. Multiplying the DC gain of the open loop response with P_1 results in the crossover frequency of the circuit arrangement of approximately $\dfrac{Z_1 g_{m1}}{(Z_1 + Z_2)C_m}$ since $C_p << C_m g_{m2} R_2$. Further the circuit arrangement has a non-dominant pole at $\dfrac{A_2}{C_L R_2} = \dfrac{g_{m2} R_2}{C_L R_2} = \dfrac{g_{m2}}{C_L}$, which relates to a barrier frequency or maximum achievable bandwidth. The dominant pole has been

reduced by approximately $C_m g_{m2} R_2 R_1$. The non-dominant pole has been increased by approximately $\dfrac{g_{m2}}{R_2}$. As a result, the dominant pole moves to a lower frequency while the non-dominant pole moves to a higher frequency.

[0010]   While the Miller compensation capacitor C_m increases the bandwidth of the two stage amplifier, additional increases in bandwidth are very difficult to achieve. Increasing the bandwidth involves moving the location of the poles, which are typically in the form of $\dfrac{1}{RC}$. The value of the parasitic capacitance C_p of the second amplifier stage cannot be reduced. The value of the resistance R_1 usually cannot be reduced without adversely impacting the gain of the first amplifier stage since $A_1 = g_{m1} R_1$ and the DC gain of the open loop response.

[0011]   Other performance criteria of multistage amplifiers include slew time, settling time and voltage rejection in power supply implementations. Referring now to FIGs. 5-7, slew time refers to the amount of time that is required for the output voltage to transition within a predetermined percentage of a final value after a change in the input voltage. The settling time refers to the amount of time that is required after the slew time for the output voltage to settle within a predetermined percentage of the final value. FIG. 6 shows exemplary slew and settling times.

[0012]   In a power supply circuit 50 that is shown in FIG. 7, one end of a Miller compensation capacitor C_m is connected to an output of the first amplifier stage 20 and an input or gate of the second amplifier stage 22. The second

amplifier stage 22 is implemented using a PMOS transistor 52 having drain that is connected to a voltage potential V_{sup}. The source of the transistor 52 is connected to an opposite end of the Miller capacitor C_m. A current source 54 and the load capacitor C_L are connected to the source of the transistor 52 as well. The transistor 52 may be implemented using other transistor technologies.

[0013]   In the circuit in FIG. 7, the slew time of the power supply circuit 50 is dependent upon the charging time of the Miller capacitance C_m. More particularly, $slewt = \dfrac{V_i C_m}{I_i}$. The slew time is proportional to the charging time for the Miller capacitance C_m, which is not desirable.

[0014]   At low frequencies, the Miller capacitance C_m is an open circuit and a feedback signal is fed back to the non-inverting input. At high frequencies, C_m shorts and a voltage divider is created between the load impedance Z_L and the transconductance g_{m2}. As a result, the output voltage $V_O = \dfrac{V_{sup} Z_L}{Z_L + \dfrac{1}{g_{m2}}}$.

Therefore, V_O is proportional to V_{sup}. The power supply has relatively poor power supply voltage rejection since the fluctuations of the supply voltage V_{sup} are also seen in the output voltage V_O.

SUMMARY OF THE INVENTION

[0015]   A compensation circuit for an amplifier with at least first and second amplifier stages comprises a first capacitance having one end that communicates with an input of the first amplifier stage. An amplifier has a first

gain, an input that communicates with an opposite end of the first capacitance, and an output. A second capacitance has a first end that communicates with the output of the broadband amplifier and an opposite end that communicates with an input of the second amplifier stage.

[0016]   In other features, the amplifier is a broadband amplifier. The broadband amplifier includes a current source and a transimpedance amplifier having an output and an input that communicates with the current source.

[0017]   In yet other features, the current source includes a first transistor including a control terminal and first and second terminals. A bias resistance has one end that communicates with the control terminal of the first transistor and an opposite end that communicates with the first terminal of the first transistor. A current source communicates with the first terminal.

[0018]   In still other features, the transimpedance amplifier includes a first transistor having a control terminal and first and second terminals. A feedback resistance has one end that communicates with the control terminal and an opposite end that communicates with the first terminal. A current source communicates with the first terminal.

[0019]   In yet other features, a buffer has an input that communicates with the output of the amplifier and an output that communicates with the one end of the second capacitance. The buffer includes a first transistor having a control terminal and first and second terminals. A second transistor has a control terminal, a first terminal that communicates with the second terminal of the first transistor, and a second terminal. Third, fourth, and fifth transistors each have a

control terminal and first and second terminals. The control terminal of the third transistor communicates with the control terminal of the second transistor. The first terminal of the third transistor communicates with the control terminal of the fourth transistor. The first terminal of the fourth transistor communicates with the control terminal of the fifth transistor. The first terminal of the first transistor communicates with the first terminal of the fifth transistor. A resistance has one end that communicates with the first terminal of the third transistor and an opposite end that communicates with the first terminal of the fourth transistor. A feedback capacitance has one end that communicates with the first terminal of the first transistor and an opposite end that communicates with the control terminals of the second and third transistors.

[0020]   In other features, an amplifier circuit comprises the compensation circuit and further comprises the first amplifier stage and the second amplifier stage.

[0021]   In still other features, a load capacitance has one end that communicates with an output of the second amplifier stage. A first impedance has one end that communicates with the input of the first amplifier stage. A second impedance has one end that communicates with the input of the first amplifier stage and an opposite end that communicates with the output of the second amplifier stage. The first and second impedances are at least one of a resistance, a capacitance and a short circuit.

[0022]   A broadband inverter comprises a first transistor having a control terminal and first and second terminals. A second transistor has a control

terminal, a first terminal that communicates with the second terminal of the first transistor, and a second terminal. Third, fourth, and fifth transistors each have a control terminal and first and second terminals. The control terminal of the third transistor communicates with the control terminal of the second transistor. The first terminal of the third transistor communicates with the control terminal of the fourth transistor. The first terminal of the fourth transistor communicates with the control terminal of the fifth transistor. The first terminal of the first transistor communicates with the first terminal of the fifth transistor. A resistance has one end that communicates with the first terminal of the third transistor and an opposite end that communicates with the first terminal of the fourth transistor. A feedback capacitance has one end that communicates with the first terminal of the first transistor and an opposite end that communicates with the control terminals of the second and third transistors.

[0023]   In other features, the first transistor is a PMOS transistor, the control terminal of the first transistor is a gate, the first terminal of the first transistor is a source and the second terminal of the first transistor is a drain.

[0024]   In other features, the second, third, fourth and fifth transistors are NMOS transistors, the control terminals of the second, third, fourth and fifth transistors are gates, the first terminals of the second, third, fourth and fifth transistors are sources and the second terminals of the second, third, fourth and fifth transistors are drains.

[0025]   In still other features, first, second, third, and fourth current sources communicate with the first terminals of the first, third, fourth and fifth transistors.

[0026]   In still other features, the control terminal of the first transistor receives an input voltage and an output voltage is produced at the first terminal of the fifth transistor.

[0027]   Further areas of applicability of the present invention will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples, while indicating the preferred embodiment of the invention, are intended for purposes of illustration only and are not intended to limit the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028]   The present invention will become more fully understood from the detailed description and the accompanying drawings, wherein:

[0029]   FIG. 1 is an electrical schematic of an amplifier circuit according to the prior art;

[0030]   FIG. 2A is an electrical schematic of a two stage amplifier circuit with a Miller compensation capacitor according to the prior art;

[0031]   FIG. 2B is an electrical schematic of an open loop response configuration of a two stage amplifier circuit with Miller compensation capacitor, internal resistances and a parasitic capacitance according to the prior art;

[0032]   FIG. 3 illustrates the open loop response of the circuit of FIG. 2A without the Miller compensation capacitor;

[0033]   FIG. 4 illustrates the open loop response of the circuit of FIG. 2A with the Miller compensation capacitor;

[0034]   FIGs. 5 and 6 illustrate an input voltage, an output voltage, slew time and settling time;

[0035]   FIG. 7 is an electrical schematic of a power supply including a two stage amplifier circuit and a Miller compensation capacitor according to the prior art;

[0036]   FIG. 8 is an electrical schematic of a two stage amplifier circuit with a compensation circuit according to the present invention;

[0037]   FIG. 9 is the electrical schematic of FIG. 8 redrawn to illustrate the feedback loop provided by the compensation circuit;

[0038]   FIG. 10 illustrates the open loop response of the circuits shown in FIGs. 8 and 9;

[0039]   FIG. 11 is an electrical schematic of a power supply including a two stage amplifier circuit and a compensation circuit according to the present invention;

[0040]   FIGs. 12A-12D illustrate various implementations of the broadband amplifier of FIG. 8;

[0041]   FIG. 13 illustrates a first implementation of the broadband buffer of FIG. 8;

[0042]   FIG. 14 illustrates a second implementation of the broadband buffer according to the present invention;

[0043]   FIG. 15 illustrates the broadband buffer circuit of FIG. 14 in an open loop response configuration; and

[0044]   FIG. 16 illustrates the open loop response of the broadband buffer circuit in FIG. 15.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0045]   The following description of the preferred embodiment(s) is merely exemplary in nature and is in no way intended to limit the invention, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify similar elements.

[0046]   Referring now to FIG. 8, a compensation circuit according to the present invention is shown for an amplifier circuit that includes two or more stages. The amplifier 16 is shown to include the first amplifier stage 20 having a first transconductance g_{m1} and the second amplifier stage 22 having a second transconductance g_{m2}. The internal resistances R_1 and R_2 and a parasitic capacitance C_p of the second amplifier stage 22 are shown. The load capacitance C_L is connected to the output of the second amplifier stage 22.

[0047]   The compensation circuit 100 includes an input capacitance C_i 110 having one end that is coupled to the inverting input of the first amplifier stage 20. An opposite end of the input capacitance C_i 110 is connected to an amplifier 114 having a gain A. In one implementation, the amplifier 114 is a

broadband amplifier. An output of the amplifier 114 is connected to an input of an optional buffer 118. An output of the buffer 118 is connected to one end of an output capacitance C_O 124. An opposite end of the output capacitance C_O is connected to the output of the first amplifier stage 20. The capacitances C_i and C_O act as a low frequency decoupler and a high frequency connector.

[0048]   Referring now to FIGs. 8 and 9, at low frequency, the capacitances C_i and C_O (110 and 124) are open circuits and the compensation circuit 100 does not provide feedback. Therefore, the compensation circuit 100 does not impact the resistance R_1 at low frequencies, which allows the amplifier to maintain a relatively high open loop DC gain. At mid to higher frequencies, the compensation circuit 100 begins providing feedback from the output of the second amplifier 22 through the impedance Z_2 and the compensation circuit 100 to the input of the second amplifier stage 22. This feedback loop can be seen more readily in FIG. 9.

[0049]   Referring now to FIG. 10, to derive the bandwidth of the circuit in FIG. 8, the open loop response technique is used as previously described. The DC gain of the open loop response is $\dfrac{Z_1}{Z_1 + Z_2} g_{m1} R_1 g_{m2} R_2$. The amplifier circuit has a dominant pole at $\dfrac{1}{C_L R_2}$. The crossover frequency of the amplifier circuit of $\dfrac{Z_1}{Z_1 + Z_2} g_{m2} A \dfrac{\dfrac{C_O}{(C_O + C_p)}}{C_L}$. Further the amplifier circuit has a non-

dominant pole at $\dfrac{g_{mbuf}}{\left(\dfrac{C_O C_p}{C_O + C_p}\right)}$, which relates to a barrier frequency or maximum

achievable bandwidth. When the compensation circuit 100 is active at mid to higher frequencies, the resistance R_1 decreases and is equal to

$$R_1' = \frac{C_L}{g_{m2} A (C_O + C_p)}.$$ Likewise, the resistance R_2 decreases and is equal to

$$R_2' = \frac{C_O}{g_{m2} A (C_O + C_p)}.$$

[0050]   The bandwidth of the amplifier has two distinct sections. The first section is dominated by the first amplifier stage 20. As the non-dominant pole of the first stage becomes problematic, the compensation circuit 100 provides feedback, which increases the bandwidth of the amplifier circuit.

[0051]   As can be appreciated, the DC gain of the amplifier is the same as the amplifier with the Miller compensation capacitor. The bandwidth of the amplifier circuit is higher by at least the gain of the amplifier 114. The bandwidth of the amplifier circuit is dependent on the transconductance of the second stage and the output capacitance C_L.

[0052]   Referring now to FIG. 11, a power supply circuit 150 includes the compensation circuit 100. The slew time is no longer dependent upon the charging time of the Miller compensation capacitor. The slew time is dependent upon the charging time of the effective capacitance of C_p combined with C_o, which is much shorter than the charging time for the Miller compensation capacitor C_m. In addition, the power supply circuit 10 exhibits improved voltage

rejection since $V_o = \dfrac{V_{sup}}{A}$. Therefore, the voltage rejection of the power supply

circuit 150 is improved by a factor of the gain A.

[0053]   The broadband amplifier 114 preferably has high gain and high

bandwidth. The broadband amplifier 114 can be implemented using a wide

variety of circuits, some of which are illustrated in FIGs. 12A-12D. Referring now

to FIG. 12A, the broadband amplifier 114-1 is shown to include a current source

160-1 and a transimpedance amplifier 164-1. As can be seen in FIG. 12B, a

transimpedance amplifier 164-2 of a broadband amplifier 114-2 can be

implemented using an operational amplifier (opamp) 166 and a feedback

resistance R_f, which is connected to the input and output of the opamp 166.

[0054]   Referring now to FIG. 12C, an alternate and presently preferred

implementation of the broadband amplifier 114-3 is shown to include a current

source 160-3 and a transimpedance amplifier 164-3. The current source 164-3

includes a transistor 170 having a gate, a source and a drain. A bias resistance

R_{bias} is connected between the gate and the drain of the transistor 170. The

drain of the transistor 170 is biased by a current source 174, which is referenced

to a supply voltage V_{dd}.

[0055]   The transimpedance amplifier 164-3 includes a transistor 176

having a gate coupled to the drain of the transistor 170. A feedback resistance

R_f has one end that is connected to the drain of the transistor 170 and an

opposite end that is connected to the drain of the transistor 176. The drain of the

transistor 176 is biased by a current source 178, which is referenced to a supply

voltage V_{dd}. In one implementation, the transistors 170 and 176 are NMOS transistors, although other transistor types may be used.

[0056]   Referring now to FIG. 12D, a broadband amplifier 114-4 is shown to include a current source 160-4 and a transimpedance amplifier 164-4. The transimpedance amplifier 164-4 includes first, second and third transistors 180, 182 and 184. The current source 160-4 biases a gate of the first transistor 180. The drain of the transistor 180 is connected to a gate of the transistor 182 and to one end of a resistance R, which has an opposite end that is connected to a drain of the transistor 182. The drain of the transistor 182 is connected to a gate of the transistor 184. The output voltage V_o is referenced from the drain of the transistor 184. The drains of the transistors 180, 182 and 184 are biased by current sources 186, 188, and 190, respectively, which are referenced to a supply voltage V_{dd}. A feedback resistance R_f has one end that is connected to the gate of the transistor 180 and an opposite end that is connected to the drain of the transistor 184. As can be appreciated by skilled artisans, there are still other ways of implementing the broadband amplifier 114 that are well within the scope of the present invention.

[0057]   Referring now to FIG. 13, the broadband inverter 118 preferably has a unitary gain and a relatively high bandwidth. One exemplary broadband inverter 118-1 is shown to include a transistor 200 having a gate that is coupled to a voltage input V_{in}. A source of the transistor 200 is biased by a current source 204, which is referenced to a supply voltage V_{dd}. The source is also

coupled to the capacitances C_o and C_p as shown. The transistor 200 can be a PMOS transistor, although other transistor types may be used.

[0058] Referring now to FIG. 14, while the broadband inverter 118-1 in FIG. 13 has satisfactory bandwidth, the presently preferred broadband inverter 118-2 in FIG. 14 has increased bandwidth. The broadband inverter 118-2 includes a first transistor 220 having a gate that receives an input voltage V_{in}. The source of the transistor 220 is coupled to a current source 224, which is referenced to a voltage supply V_{dd}. In one embodiment, the transistor 220 is a PMOS transistor, although other transistor types may be used. A drain of the transistor 220 is connected to a drain and a gate of a transistor 226 and a gate of a transistor 230, which has a transconductance g_{m1}.

[0059] A drain of the transistor 230 is biased by a current source 232, which is referenced to a supply voltage V_{dd}. The drain of the transistor 230 is also connected to a gate of a transistor 234 (which has a transimpedance g_{m2}) and one end of a resistance R. An opposite end of the resistance R is connected to a drain of the transistor 234. The drain of the transistor 234 is biased by a current source 236, which is referenced to a supply voltage V_{dd}. The drain of the transistor 234 is also connected to the gate of a transistor 238, which has a transconductance g_{m3}. The drain of the transistor 238 is biased by a current source 240, which is referenced to a supply voltage V_{dd}. The drain of the transistor 238 is connected to the source of the transistor 220 and to capacitances C_o and C_p. A feedback capacitance C_f is connected between the source of the transistor 220 and the gates of the transistors 226 and 230.

[0060]   Referring now to FIGs. 15 and 16, the bandwidth of the broadband inverter 118-2 can be found using the open loop response technique that was described above. In FIG. 15, the feedback loop is opened and a voltage source V_{in} is connected to one end of the opened feedback loop. The output voltage V_o is taken at the other end of the opened feedback loop. Parasitic capacitances C_1, C_2 and C_3 are shown and are located at the gates of the transistors 230, 234, and 238.

[0061]   The input voltage V_{in} generates a current $I_1 = V_{in}g_{mp}$. I_1 is mirrored and generates a voltage $V_2 = V_{in}g_{mp}R_f$. A current I_3 is produced that is equal to V_2g_{m3}. The output voltage V_o is equal to I_3R_{o3}, where R_{o3} is the output resistance of the transistor 238. Substituting for I_3 and then for V_2 in the equation for V_o and dividing by V_{in} yields the DC gain for the open loop response of $g_{mp}R_fg_{m3}R_{o3}$. A dominant pole is located at $\dfrac{1}{R_{o3}C_{Leff}}$, where C_{Leff} is equal to a series connection of C_o and C_p. Therefore, multiplying the DC gain of the open loop response and the dominant pole yields a crossover frequency at $\dfrac{g_{mp}R_fg_{m3}}{C_{Leff}}$.

[0062]   Without the feedback capacitance C_f, this circuit would have non-dominant poles at $\dfrac{g_{mp}}{C_{gmp}}$ (where C_{gmp} is the parasitic capacitance of the transistor 220), $\dfrac{g_{m1}}{C_1}$, $\dfrac{g_{m2}}{C_2}$, and $\dfrac{g_{m3}}{C_3}$. Since these non-dominant poles occur at approximately the same frequency F, the parallel combination of these four poles

creates a non-dominant pole at $\dfrac{F}{4}$. These non-dominant poles create a barrier

frequency that is relatively low.

[0063]   By connecting the capacitance C_f as shown in FIGs. 14 and 15,

the effect of two of the poles $\dfrac{g_{mp}}{C_{gmp}}$ and $\dfrac{g_{ml}}{C_l}$ is eliminated and the frequency of

the non-dominant poles increases to $\dfrac{F}{2}$, which is a higher barrier frequency. As

can be appreciated by skilled artisans, there are still other ways of implementing

the broadband inverter 118 that are well within the scope of the present

invention.

[0064]   Those skilled in the art can now appreciate from the foregoing

description that the broad teachings of the present invention can be implemented

in a variety of forms.   While a non-differential architecture is shown, skilled

artisans will appreciate that the present invention applies to differential circuits as

well. Therefore, while this invention has been described in connection with

particular examples thereof, the true scope of the invention should not be so

limited since other modifications will become apparent to the skilled practitioner

upon a study of the drawings, the specification and the following claims.